

## IN THE CLAIMS

1. (Currently amended) A method of power management in a digital processing apparatus, the method comprising: receiving a free-running master clock signal; and generating a plurality of sub-clocking signals from said master clock signal, wherein said plurality of sub-clocking signals change from a power-up rest condition to a ~~free running~~continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).

2. (Currently amended) A device for power management for a digital processing apparatus, the device comprising: means (10, 20) for receiving a ~~free running~~continuously free running master clock signal; and means (10, 20) for generating a plurality of sub-clocking signals from said master clock signal, wherein said plurality of sub-clocking signals change from a power-up rest condition to a ~~free running~~continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).

3. (Currently amended) A device according to claim 2, wherein each sub-clocking signal is used to clock a separate data processing part (30<sub>0</sub>-30<sub>3</sub>) of said apparatus (30).

4. (Currently amended) A device according to claim 3, wherein each data processing part (30<sub>0</sub>-30<sub>3</sub>) comprises circuitry for processing a particular serial data bit or bits of a data word.

5. (Currently amended) A device according to claim 4, wherein said digital signal processing apparatus has a particular maximum data width and wherein said plurality of sub-clocking signals corresponds to said maximum data width.

6. (Currently amended) A device according to claim 2, wherein during a switch-off phase of said digital processing apparatus, said plurality of sub-clocking signals change from a ~~free running~~continuously free running condition to a rest condition one

at a time.

7. A device according to claim 2, wherein said means for receiving a master clocking signal and generating a plurality of sub-clocking signals comprise: a shift register (10) for providing a plurality of enabling signals, said plurality of enabling signals each changing from a non-active rest condition to an active normal condition and thereafter remaining at said active normal condition, said plurality of enable signals changing from the rest condition to the normal condition one at a time at predetermined time intervals following the initial switch on; and logic circuitry (20) for receiving the enable signals and sequentially enabling the production of the sub-clocking signals.

8. A device according to claim 7, wherein the logic circuitry (20) comprises means (22<sub>0</sub>-22<sub>3</sub>) for ANDing respective enable signals with the master clock.

9. A device according to claim 8, wherein the logic circuitry (20) comprises a number of AND gates (22<sub>0</sub>-22<sub>3</sub>) corresponding to the number of enable signals, each AND gate (22<sub>0</sub>-22<sub>3</sub>) having a first input (24<sub>0</sub>-24<sub>3</sub>) for receiving its respective enable signal and a second input (26<sub>0</sub>-26<sub>3</sub>) for receiving the master clocking signal, said sub-clocking signals being produced at the respective outputs of said AND gates.

10. Digital processing apparatus comprising: a device in accordance with claim 2, and a plurality of discrete data processing parts, each of said data processing parts being clocked by a respective one of said plurality of sub-clocking signals.